EE 435
Laboratory Experiment 2
Spring 2025

Operational Amplifier Design

The operational amplifier is one of the most widely used analog circuits with virtually all analog and mixed-signal circuit designers being expected to be knowledgeable about both the design and operation of the operational amplifier. Although the concept of the operational amplifier is very fundamental and although there have been a very large number of operational amplifiers designed by a large number of engineers, the design of operational amplifiers continually presents challenges even to experienced designers.

In this experiment, emphasis will be placed on the design of the most basic operational amplifier, a single-stage amplifier with differential inputs and a single-ended output using a tail-current bias. This basic structure can be systematically derived from either an n-channel or a p-channel quarter circuit. The structure of this amplifier, based upon the n-channel quarter circuit is shown in Fig. 1 where the transistor M_9 has been used to generate the tail-current bias.

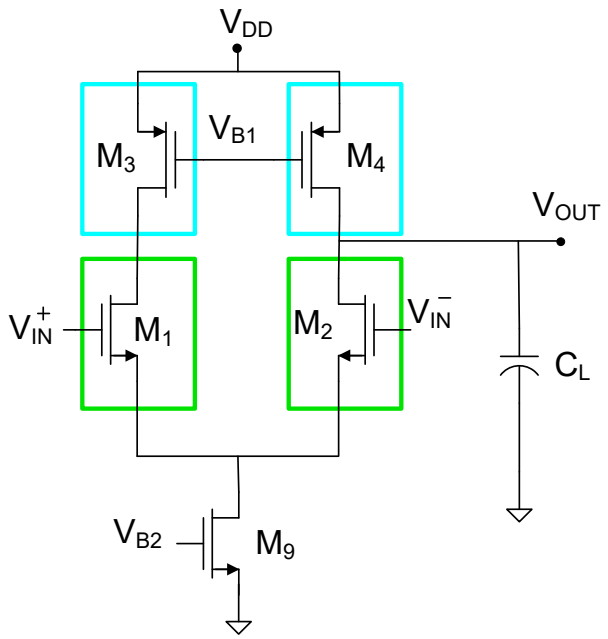

Fig. 1. Basic Operational Amplifier

Although this circuit will work fine for the appropriate value of bias voltage V_{B1}, a common-mode feedback circuit (CMFB) is generally required to generate this bias voltage and there is modest circuit overhead associated with the CMFB biasing circuit. These will be discussed later in the course.

Since it will be assumed in this experiment that only a single-ended output is being used on this circuit, the voltage on the drain node of M_1 is not critical and it can be shown that this node can be used to bias M_3 and M_4 without requiring a CMFB. The

modified version of this amplifier is shown in Fig. 2 where the gates of M_3 and M_4 are connected so as to form a current mirror that mirrors the current in M_3 to that in M_4.

.

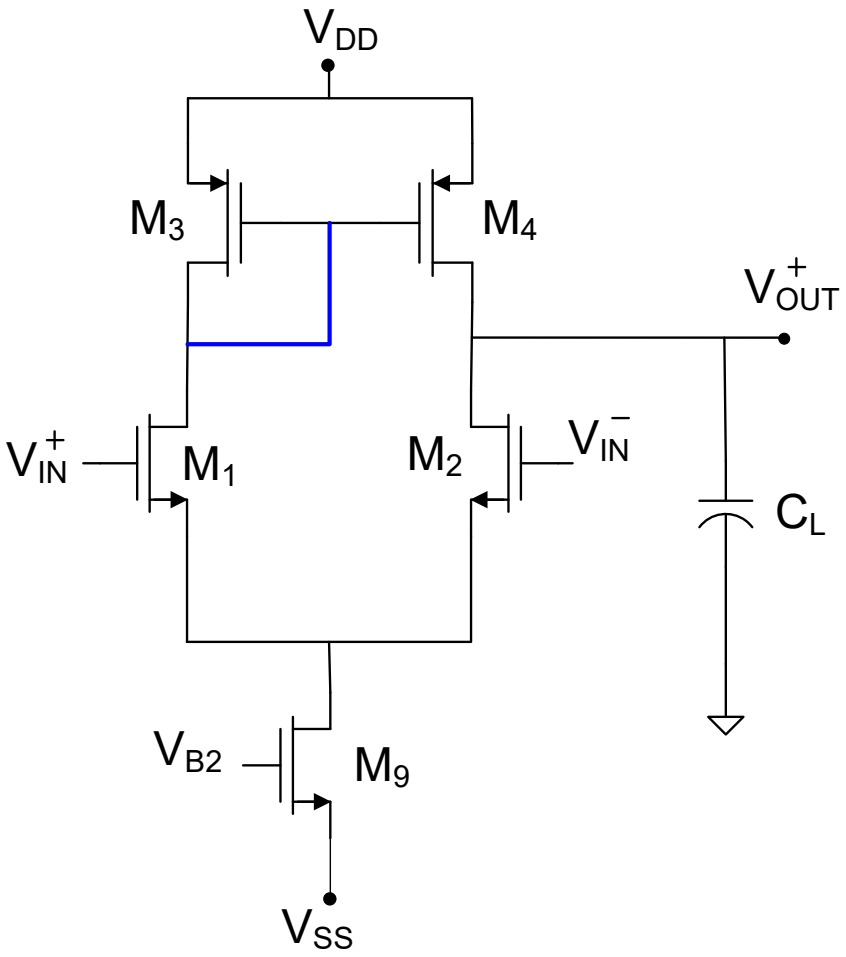

Fig. 2 Basic Operational Amplifier with Current-Mirror Biasing

Our goal in this experiment will be to design an operational amplifier based upon this architecture and to compare the theoretical values for some of the key performance parameters of this structure with that obtained in a theoretical analysis. In this design, it will be assumed that the TSMC 0.18μ CMOS process is to be used, the supply voltages V_{DD} and V_{SS} are fixed at +1.3V and -1.3V respectively, the excess bias voltage V_{B2} is fixed at 0.3V, and the capacitor C_L is given. It will be assumed that the quiescent input voltages are both 0V and the desired quiescent output voltage is also 0V though the amplifier can be operated over some range of common-mode input and quiescent output values.

Consistent with the concept of symmetric circuits, it will be assumed that the circuit will be designed under the assumption that matching between the left-half and the right-half circuits is to be maintained.

Part 1 Determine the number of degrees of freedom in this design and list the design variables.

Part 2 Design an operational amplifier using the architecture of Fig. 2 that can drive a capacitive load of 10pF using an analytical formulation for the amplifier. This design should result in determining all of the natural design parameters for this circuit. The amplifier should have a GB of at least 10MHz , a dc voltage gain of at least 100 when driving this load, and a p-p output swing of 0.5V for some common-mode input levels and some quiescent output level.

Part 3 Simulate the amplifier you designed in Part 2 in Specrtre using the TSMC 0.18μ CMOS process. Compare the dc gain, the GB, the output signal swing, and the SR with what you obtained by the analytical formulation.

Part 4 Make minor changes, if necessary, in the design so that the simulated performance meets the design requirements. Verify by computer simulations that the performance requirements have been met.

Part 5 Layout the circuit that you have designed and compare the post-layout extracted performance with that of your circuit schematic. Resolve the reasons for any discrepancies between the original schematic simulation and that of the extracted circuit.